

CDA 3101: Introduction to Computer Hardware and Organization

Fall Term, 1999

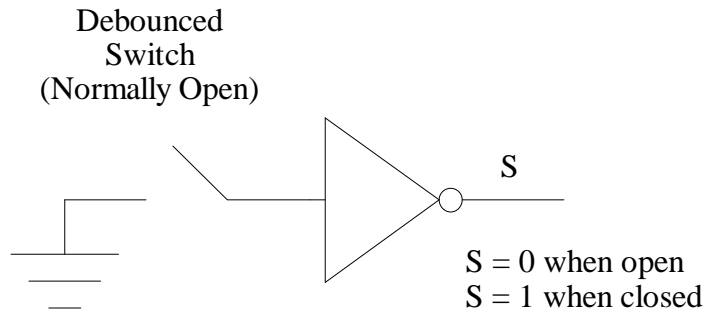
Lab 2: Sequential Logic Circuits:

Due Dates:

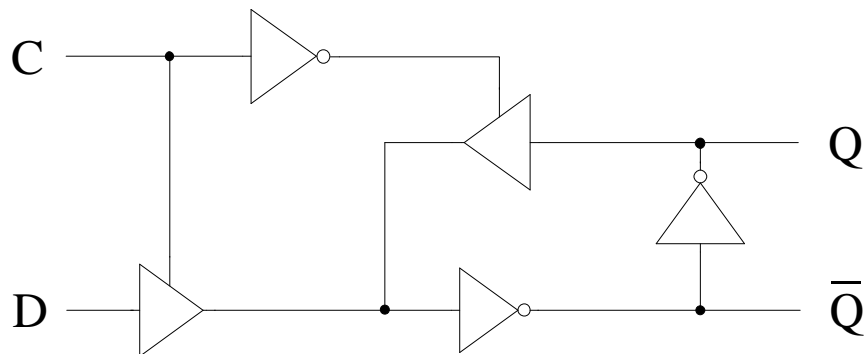
Section 043 - Monday, October 18, 1999 (beginning of class)

Section 044 - Tuesday, October 19, 1999 (beginning of class)

- A. Using NAND gates, implement an SR latch with control (or enable, see page 124). Also implement an \overline{S} R latch with control using NOR gates. Convert your \overline{S} R latch into an SR latch. Hook inputs in parallel to your two latches and attach outputs to lights. Verify your two latches and compare their behavior.
- B. Modify the design of the SR latches that you created in part A to produce two (clocked) D latches (see page 125 to find out how to do this with NANDs, you should then be able to figure out how to do it with NORs). Using a debounced switch for your clock (you will need to attach an inverter to the debounced switch to produce both 0 and 1 signals) and a slide switch for the D input, hook up your two D latches in parallel (outputs as before). Verify the operation of the D latches and compare behavior.



- C. Verify the operation of the TRI-STATE buffers on a 74126 chip. Using tri-state buffers, construct the D-latch diagrammed as follows:



Hook this latch up in parallel with the two you already, verify its operation and compare behavior with the two you already have working.

- D. Connect any two of your D latches to produce a Master-Slave D flip-flop (see page 126). Attach the outputs of both master and slave to lights so that you can observe the behavior of each. Verify the operation of your D ff using a debounced switch for the clock as before. Determine if the D ff you have constructed is positive or negative edge triggered.
- E. Construct the positive-edge triggered D flip-flop as diagrammed on page 129. Again, using a debounced switch for the clock input and a slide switch for data, verify the operation of your D flip flop. Probe the behavior, via separate lights, of each of the three latches used in the construction to observe their individual behavior.
- F. Verify the operation of the two D flip flops on a 7474 chip. Hook these two ff's and the two you constructed to a single input switch and a single debounced switch for clock input. Adjusting edge-triggering as necessary, demonstrate duplicate behavior for all 4 ff's.
- G. Build a 4 bit register (parallel in, parallel out) by giving each ff in your set-up from part F its own input. Use 4 consecutive slide switches for ff inputs, and 4 consecutive lights to show register contents.

Write a report ordered as follows:

- * cover page with group number and team member signatures
- * completed certification page for each team member
- * concise problem statement stating the purpose of the exercise and how it is to be done
- * equipment explanations: equipment required and carefully explained schematic diagrams (beginning with this lab, you are no longer required to do diagrams of actual wiring).
- * technical explanations: for this lab you will need to explain your design, exhibiting and amplifying on ff function tables and explaining why each design should work as specified.
- * technical observations: recapitulation - please do not recite your implementation problems except as they lead to discovery; you are experimenting; in this lab, you have three different means of producing a clocked D latch; are there any observable differences among them? did you have excess gates you couldn't take advantage of? how might one or the other contribute to minimal chip utilization? how did internal latches used in your ff constructions behave relative to overall ff behavior? discuss tactics employed to enable mixing of positive and negative edge triggered devices ... what are possible problems? are there advantages for D vs. RS latches that you were able to determine from the lab? Did you have design alternatives? (and why did you go the way you did - you might consider the ramifications of having only JK ff's available, for example), etc.
- * technical conclusions: observations which allow you to reach definitive conclusions should be concisely summed up; for this lab, the theory says that you should be able to substitute any one of the D latches for any other; it also says a steps must be taking if you wish to mix positive and negative edge triggered devices (whether or not you observed the consequences of not taking such steps, explain). Does your experiment provide support what the theory tells us about ff's and latches? Can you make any statement regarding the relative merit of a circuit constructed with negative vs. positive edge triggered devices? (and support it from the lab).